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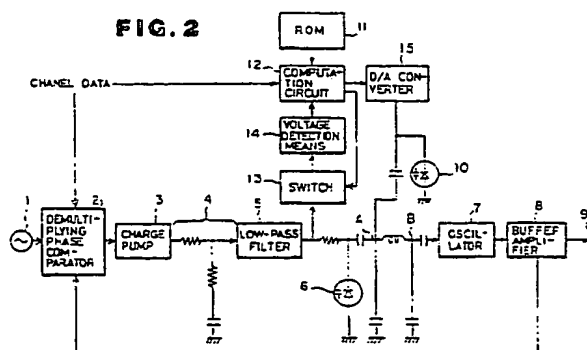
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54 Frequency Synthesizer.

57 A frequency synthesizer is designed to modify voltage value data read out of a memory means in accordance with the output voltage of a filter means, and apply a d.c. voltage corresponding to the modified data to the second variable-capacitance diode in connection with a VCO, thereby allowing the VCO frequency switching without imposing a significant fluctuation of the application voltage to the first variable-capacitance diode and accomplishing a short channel switching time and stable operation

against the temperature fluctuation. The device is further designed to supply a voltage setup value read out of the memory means to the second variable-capacitance diode thereby to reduce the frequency matching time at channel switching, and to determine such another voltage setup value as to reduce the time of phase matching based on the trend of change in the filter output voltage and supply the value to the second variable-capacitance diode.

FIG. 2



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FREQUENCY SYNTHESIZER

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a frequency synthesizer based on the phase-locked loop (will be termed PLL hereinafter) scheme.

Description of the Prior Art

Fig. 1 is a block diagram showing a conventional frequency synthesizer. In the figure, indicated by 1 is a reference signal oscillator, and 2 is a demultiplying phase comparator which compares in phase a signal derived from the output signal of the frequency synthesizer demultiplied by a factor determined by the input channel data with the reference signal provided by the reference signal oscillator 1. 3 is a charge pump which generates pulses in accordance with a phase difference signal produced by the demultiplying phase comparator 2. 4 and 5 are a lag-lead filter and a low-pass filter which function to smooth the pulses produced by the charge pump 3.

Indicated by 6 is a first variable-capacitance diode which varies in its capacitance in response to the output voltage of the low-pass filter 5, 7 is an oscillator which oscillates at a frequency determined by the capacitance of the first variable-capacitance diode 6, the variable-capacitance diode 6 and oscillator 7 in combination constituting a voltage-controlled oscillator (will be termed VCO hereinafter). 8 is a buffer amplifier for amplifying the output of the oscillator 7, and 9 is an output terminal from which the amplified output of the buffer amplifier 8 is delivered. The output signal of the buffer amplifier 8 is, at the same time, partly fed back to the demultiplying phase comparator 2.

Next, the operation of the foregoing arrangement will be explained. The output signal fed back from the buffer amplifier 8 is demultiplied by the factor specified in the channel data by the demultiplying phase comparator 2, and the result is compared in phase with the reference signal provided by the reference signal oscillator 1. The phase difference signal resulting from the phase comparison by the demultiplying phase comparator 2 is fed to the charge pump 3, which then generates pulses in accordance with the received phase difference signal and sends it to the lag-lead filter 4. The pulses generated by the charge pump 3 are smoothed by the lag-lead filter 4 and low-pass filter

5 and, after being converted into a predetermined d.c. voltage, it is applied to the first variable-capacitance diode 6.

The variable-capacitance diode 6 has its capacitance value established in correspondence to the d.c. voltage supplied from the low-pass filter 5, and the oscillator 7 oscillates at a frequency which is determined by the capacitance of the first variable-capacitance diode 6. The output of the oscillator 7 is amplified by the buffer amplifier 8, and the amplified signal is delivered from the output terminal 9 and, at the same time, fed back to the demultiplying phase comparator 2. The phase-locked loop system operates such that the phase difference revealed by the demultiplying phase comparator 2 subsides ultimately, and consequently the VCO made up of the variable-capacitance diode 6 and oscillator 7 has its oscillation frequency settled to a certain value. This state of operation is called "locked state".

The conventional frequency synthesizer, arranged as described above, needs time for frequency matching in the phase lock process, which is dependent on the time constant of the lag-lead filter 4. Therefore it cannot have a quick variation of the application voltage to the first variable-capacitance diode 6 at the switching of frequencies, resulting adversely in an excessive time consumption for channel switching, and it involves a problem of being deficient as a frequency synthesizer used in the digitized radio communications equipment in which frequency hopping is required.

An example of schemes which copes with this problem is described in Japanese Patent Unexamined Publication No. 57-160227, however, it still involves a problem of prolonged switching time due to the temperature fluctuation of the VCO.

SUMMARY OF THE INVENTION

The present invention is intended to overcome the foregoing prior art deficiency, and its prime object is to provide a frequency synthesizer which is highly responsive to frequency switching and also stable against the temperature fluctuation.

The inventive frequency synthesizer has its VCO connected with, in addition to a first variable-capacitance diode, a second variable-capacitance diode which determines the VCO frequency, and is further provided with a memory means which stores voltage value data indicative of d.c. voltages applied to the second variable-capacitance diode in accordance with the channel data, a voltage detec-

tion means which measures the output voltage of a filter means, a computation means which modifies the voltage value data read out of the memory means in accordance with the output voltage of the filter means, and a conversion means which converts the modified data provided by the computation means into a corresponding d.c. voltage and applies it to the second variable-capacitance diode.

Furthermore, the inventive frequency synthesizer has its VCO connected with, in addition to a first variable-capacitance diode, a second variable-capacitance diode which determines the VCO frequency, and is further provided with a memory means which stores voltage value data indicative of d.c. voltages applied to the second variable-capacitance diode in accordance with the channel data, a voltage detection means which measures the output voltage of a filter means, a computation means which delivers the voltage value data read out of the memory means as a voltage setting value and, thereafter, delivers another voltage setting value in accordance with the output value of the filter means, and a conversion means which converts the voltage setting value provided by the computation means into a d.c. voltage and applies it to the second variable-capacitance diode.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing the conventional frequency synthesizer;

Fig. 2 is a block diagram showing the frequency synthesizer based on the first embodiment of the present invention;

Fig. 3 is a characteristic diagram showing the relation between the control voltage and oscillation frequency of the VCO;

Fig. 4 is a waveform diagram showing the voltage applied to the first variable-capacitance diode;

Fig. 5 is a block diagram showing the frequency synthesizer based on the second embodiment of the present invention;

Fig. 6 is a block diagram showing the frequency synthesizer based on the third embodiment of the present invention; and

Fig. 7 is a block diagram showing the frequency synthesizer based on the fourth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The first embodiment of this invention will be described with reference to the drawings. In Fig. 2,

indicated by 1 is a reference signal oscillator, 2 is a demultiplying phase comparator, 3 is a charge pump, 4 is a lag-lead filter, 5 is a low-pass filter, 6 is a first variable-capacitance diode, 7 is an oscillator, 8 is a buffer amplifier, and 9 is an output terminal. These components are identical or comparable to those referred to by the same symbols in Fig. 7 and their explanation will be omitted.

The arrangement further includes a second variable-capacitance diode 10, which is connected together with the first variable-capacitance diode 6 to the oscillator 7 and functions to determine the oscillation frequency of the oscillator 7. A VCO is formed by the first variable-capacitance diode 6, second variable-capacitance diode 10, and oscillator 7. Indicated by 11 is a read-only memory (will be termed ROM hereinafter) used as a memory means for storing in advance the voltage value data for all channels indicative of d.c. voltages applied to the second variable-capacitance diode 10 at a prescribed temperature (e.g., 25°C) in accordance with the channel data. 12 is a computation circuit consisting of a microprocessor, for example, which operates to modify the voltage value data, which corresponds to the channel data retrieved from the ROM 11, in accordance with the d.c. voltage which has been provided by the low-pass filter 5 at the previous channel switching. 13 is a switch operated to conduct or block the output of the low-pass filter 5. 14 is a voltage detection means which evaluates the d.c. voltage provided by the low-pass filter 5, and it is an A/D converter in this embodiment. 15 is a D/A converter which functions to convert the data provided by the computation circuit 12 into a d.c. voltage and applies it to the second variable-capacitance diode 10.

Next, the operation of the foregoing arrangement will be explained. As in the case of the conventional arrangement, the output signal fed back from the buffer amplifier 8 is demultiplied by the demultiplying phase comparator 2 and compared in phase with the reference signal produced by the reference signal oscillator 1. In response to a phase difference provided by the demultiplying phase comparator 2, the charge pump 3 operates to generate pulses. These pulses are smoothed by the lag-lead filter 4 and low-pass filter 5, and the resulting d.c. voltage is applied to the first variable-capacitance diode 6. Upon receiving the channel data, the computation circuit 12 makes access to the ROM 11 to read out the voltage value data corresponding to the channel data and implements the prescribed computation for the voltage value data to produce modified data, which is sent to the D/A converter 15. The D/A converter 15 converts the modified data into a corresponding d.c. voltage, which is applied to the second variable-capacitance diode 10.

The first and second variable-capacitance diodes 6 and 10 have their capacitances established in correspondence to the applied d.c. voltages, and the oscillator 7 oscillates at a frequency determined by the capacitances of the variable-capacitance diodes 6 and 10. A large variation of frequency due to channel switching is accomplished by the capacitance variation of the second variable-capacitance diode 10, and the first variable-capacitance diode 6 performs fine adjustment for the switching frequency. Namely, the d.c. voltage applied to the first variable-capacitance diode 6 varies in a narrow range needed for phase matching the phase locking process, and consequently it becomes possible to have a quick channel switching without the influence of the time constant of the lag-lead filter 4.

Fig. 3 is a graphical representation of the relation between the control voltage and oscillation frequency of VCO, with the temperature being a parameter. In case it is intended to lock the VCO oscillation frequency to F_1 (MHz), the application voltage is 0.94 V at -10°C or it is 1.4 V at $+80^\circ\text{C}$, having a difference of about 0.46 V. Similarly, locking to F_2 (MHz) requires 5.22 V at -10°C or 5.85 V at $+80^\circ\text{C}$, having a difference of about 0.63 V. Since the ROM 11 stores the voltage value data calibrated to $+25^\circ\text{C}$ as mentioned previously, it releases the output corresponding to 1.11 V for the frequency locking to F_1 . If the temperature is $+80^\circ\text{C}$, the VCO initially oscillates at f_1 lower than F_1 , and thereafter the PLL operates to vary the d.c. voltage applied to the first variable-capacitance diode 6, and eventually the VCO frequency is locked to F_1 . However, before the VCO frequency is locked to F_1 , it needs some time length, which is determined from the frequency difference, and therefore the frequency difference must be minimized.

In dealing with this matter, the computation circuit 12, upon receiving the channel data, reads the corresponding voltage value data out of the ROM 11 and performs the calculation of data modification based on the previous measured value (which will be explained later). The modified data is delivered to the D/A converter 15 and, after the output voltage of the low-pass filter 5 has settled, the switch 13 is made conductive. Consequently, the d.c. voltage which is supplied from the low-pass filter 5 to the first variable-capacitance diode 6 is introduced to the A/D converter 14, which then converts the voltage into a digital value. The computation circuit 12 holds the digital value so that it is used as a measured value at the next channel switching. Accordingly, the previous measured value stands for the value of output voltage of the low-pass filter 5 measured at the previous channel switching. At channel switching, if the previous measured value is the reference value V_0 (the

voltage value for 25°C corresponding to the frequency which has been set at the previous channel switching), the computation circuit 12 delivers, as modified data, the voltage value data retrieved from the ROM 11 without any computation process. If there is a difference in the previous measured value from the reference voltage V_0 , the computation circuit 12 performs the calculation for converting the difference into a d.c. voltage to be applied to the second variable-capacitance diode 10, and delivers the resulting modified data. The characteristic diagram of Fig. 2 is assumed to present the relation between the voltage applied to the first variable-capacitance diode 6 and the output signal (the graph is not accurate in a qualitative sense, but it represents the trend). Assuming the setup frequency at the previous channel switching to be F_1 , with the reference value V_0 being 1.11 V and measured value being 1.4 V on the characteristic diagram, the temperature of VCO is inferred to be $+80^\circ\text{C}$. Further assuming the setup frequency at the present channel switching to be F_2 , the ROM 11 reads out a value corresponding to 5.50 V and a value for $+80^\circ\text{C}$, i.e., a value corresponding to 5.85 V, is supplied as modified data to the D/A converter 15. In this manner, the voltage value data read out of the ROM 11 is modified on the basis of the previous measured value, on the premise that there is no extreme temperature variation from one channel switching to the next channel switching. The computation circuit 12 holds values for -10°C and $+80^\circ\text{C}$, and the value at a temperature between these temperatures can be obtained by interpolation.

Although in the foregoing embodiment the second variable-capacitance diode 10 is connected on the side of the first variable-capacitance diode 6 as indicated by A in Fig. 2, it may be connected on the side of the oscillator 7 as indicated by B, depending on the sensitivity of the device, and the same effectiveness as of the above embodiment will be achieved.

The time length T expended by the frequency synthesizer for frequency switching is expressed by the following formula.

$$T = T_f + T_p$$

where T_f is the time length until the output signal frequency reaches the intended frequency, and T_p is the time length after the frequency settlement until the output signal is in-phase with the reference signal. The frequency synthesizer of the foregoing embodiment is effective for the reduction of T_f . However, after the output signal has reached the intended frequency in response to the voltage output to the second variable-capacitance diode 10, the frequency synthesizer attempts to make phase matching by temporarily shifting the frequency of the output signal. Therefore, as shown in Fig. 4 the

voltage applied to the first variable-capacitance diode 6, i.e., the output voltage of the low-pass filter 5, has a fluctuation after a prescribed voltage has been applied to the second variable-capacitance diode 10. The time length since the voltage change has begun until the frequency is locked is T_p . By reducing even this phase-in time T_p , the time expended for frequency switching can further be reduced.

Fig. 5 is a block diagram having the frequency synthesizer based on the second embodiment of this invention which is intended to reduce even the phase-in time T_p . In the figure, indicated by 22 is a computation circuit which delivers the voltage value data read out of the ROM 11 in correspondence to the channel data directly to the D/A converter 15 and delivers the voltage setup value determined based on the output voltage of the lag-lead filter 4 to the D/A converter 15. 23 is a switch, and 24 is an A/D converter which converts the output voltage of the lag-lead filter 4 into a digital value.

Next, the operation of the above arrangement will be explained. In response to the entry of channel data at channel switching, the computation circuit 22 reads the voltage value data corresponding to that channel data out of the ROM 11, which is delivered to the D/A converter 15. The D/A converter 15 converts the voltage value data into an analog voltage, which is applied to the second variable-capacitance diode 10. Consequently, the oscillator 7 produces a frequency corresponding to the channel.

However, the output signal is generally out of phase with the reference signal, and the demultiplying phase comparator 2 produces a phase difference signal. The lag-lead filter 4 has its output voltage varying in response to the phase difference signal (refer to Fig. 3). Subsequently, the computation circuit 22 brings the switch 23 conductive. Then, the output voltage of the lag-lead filter 4 is converted into a digital value by the A/D converter 24, which is received by the computation circuit 22. Based on the digital value, the computation circuit 22 can recognize whether the PLL system is going to raise or lower the frequency of the output signal. In case the lag-lead filter 4 has a rising output voltage, the PLL system is operating for phase matching through a rise in the output frequency of the oscillator 7. In this case, the computation circuit 22 provides a value larger than the existing voltage value data for the D/A converter 15, resulting in a rise in the output frequency of the oscillator 7. If the rise of the output voltage of the lag-lead filter 4 is sharp, an increased value may be provided for the D/A converter 15. Conversely, in case the lag-lead filter 4 has a falling output voltage, a value smaller than the existing voltage value data is set to the D/A converter 15.

In this manner, the computation circuit 22 swiftly detects the trend of frequency variation of the oscillator 7 implemented by the PLL system to pull-in the phase thereby to apply a voltage which accords with the detected situation to the second variable-capacitance diode 10 by way of the D/A converter 15, whereby the output frequency of the oscillator 7 can be varied swiftly. Consequently, the time length for bringing the output signal in-phase with the reference signal is reduced. The switch 23 is made nonconductive when the phase matching completes, i.e., at the time of phase lock.

The output voltage of the filter means may be led out at the output of the low-pass filter 5, or more preferably it is the output of the lag-lead filter 4 which is located more front in order to detect the output trend of the filter means more swiftly.

Fig. 6 is a block diagram showing the frequency synthesizer based on the third embodiment of this invention, in which the switch 13 and A/D converter 14 shown in Fig. 1 are added to the arrangement of Fig. 5. In the figure, indicated by 32 is a computation circuit which functions as both of the computation circuit 12 in Fig. 1 and the computation circuit 22 in Fig. 4.

Next, the operation of this frequency synthesizer will be explained. The computation circuit 32 responds to the entry of channel data at channel switching to implement the modification based on the previous measured value for the voltage value data read out of the ROM 11, as in the first embodiment, and thereafter it delivers the modified data to the D/A converter 15. Subsequently, the computation circuit 32 brings the switch 23 conductive so as to introduce the output voltage value from the lag-lead filter 4, as in the second embodiment. The computation circuit 32 provides a new voltage setup value in compliance with the output voltage value to the D/A converter 15. Consequently, the output signal is rendered a swift frequency matching and phase matching without being affected by the fluctuation of the VCO temperature.

Fig. 7 is a block diagram showing the frequency synthesizer based on the fourth embodiment of this invention, in which a temperature sensor 46 is provided for measuring the ambient temperature of the VCO. The ROM 41 stores voltage value data applied to the second variable-capacitance diode 10 in correspondence to all channel data and to extensive VCO temperatures. The computation circuit 22 responds to the entry of channel data at channel switching to read the voltage value data for that channel data out of the ROM 11. Through the provision of the wiring from the outputs of the temperature sensor 46 (indicative of the immediate temperature) to the address bits of the ROM 11, the computation circuit 22 receives the voltage value data corresponding to then tem-

perature and channel data, allowing the circuit 22 to deliver the voltage value data directly to the D/A converter 15. The subsequent operation is identical to the third embodiment. This arrangement achieves the same effectiveness as of the third embodiment without the need of the A/D converter 14 which serves as a voltage detection means.

According to this invention, as described above, the frequency synthesizer is arranged such that the VCO is connected with the second variable-capacitance diode which has the application of a d.c. voltage that accords with the modified data based on the output voltage of a filter means derived from the voltage value data read out of the memory means in accordance with the channel data, allowing the VCO to have a frequency switching without causing a significant fluctuation of the application voltage to the first variable-capacitance diode, whereby the channel switching time can be reduced and the frequency synthesizer operates stably against the temperature variation.

According to this invention, the frequency synthesizer is arranged such that the VCO is connected with the second variable-capacitance diode which has the application of a d.c. voltage that accords with the voltage value data read out of the memory means in accordance with the channel data, and subsequently a d.c. voltage which accords with another voltage value depending on the output voltage of a filter means is applied to the second variable-capacitance diode, allowing the VCO to have a swift frequency switching and a reduced time length needed for the phase matching between the output signal and reference signal, whereby the frequency synthesizer has a reduced channel switching time.

Claims

1. A frequency synthesizer comprising a reference signal oscillator which generates a reference signal; a demultiplying phase comparator which compares a signal, that is derived from the output signal through demultiplication by a factor determined by channel data, with the reference signal provided by said reference signal oscillator; a filter means which smoothes the output of said demultiplying phase comparator; a first variable-capacitance diode which varies in the capacitance thereof in response to the output voltage of said filter means; and an oscillator which oscillates at a frequency determined from the capacitance of said first variable-capacitance diode to produce said output signal, wherein said oscillator is connected with said first variable-capacitance diode and a second variable-capacitance diode which determines the oscillation frequency of said oscillator, and wherein said fre-

quency synthesizer further comprises:

a memory means which stores voltage value data indicative of d.c. voltages to be applied to said second variable-capacitance diode in accordance with said channel data;

a voltage detection means which measures the output voltage of said filter means;

a computation means which modifies voltage value data read out of said memory means in accordance with the output value of said voltage detection means thereby to produce modified data; and

a conversion means which converts the modified data provided by said computation means into a d.c. voltage and applies the resulting d.c. voltage to said second variable-capacitance diode.

2. A frequency synthesizer according to claim 1, wherein said memory means stores, for all channels, voltage value data corresponding to voltages to be applied to said second variable-capacitance diode at a certain temperature.

3. A frequency synthesizer according to claim 2, wherein said computation means holds the output voltage value of said filter means which has been introduced at the previous channel switching, and produces modified data to be used for the present channel switching from the output voltage value that has been held and voltage value data which is read out of said memory means.

4. A frequency synthesizer according to claim 3, wherein said computation means produces modified data which is larger than the voltage value data read out of said memory means if the output voltage value that has been held is larger than a certain reference value, or produces modified data which is smaller than said voltage value data if the output voltage value that has been held is smaller than a certain reference value.

5. A frequency synthesizer comprising a reference signal oscillator which generates a reference signal; a demultiplying phase comparator which compares a signal, that is derived from the output signal through demultiplication by a factor determined by channel data, with the reference signal provided by said reference signal oscillator; a filter means which smoothes the output of said demultiplying phase comparator; a first variable-capacitance diode which varies in the capacitance thereof in response to the output voltage of said filter means; and an oscillator which oscillates at a frequency determined from the capacitance of said first variable-capacitance diode to produce said output signal, wherein said oscillator is connected with said first variable-capacitance diode and a second variable-capacitance diode which determines the oscillation frequency of said oscillator, and wherein said frequency synthesizer further comprises:

a memory means which stores voltage value data indicative of d.c. voltages to be applied to said

second variable-capacitance diode in accordance with said channel data.

a voltage detection means which measures the output voltage of said filter means;

a computation means which delivers voltage value data read out of said memory means as voltage setup value and, thereafter, produces an voltage setup value in accordance with the output value of said voltage detection means; and

a conversion means which converts the voltage setup value provided by said computation means into a d.c. voltage and applies the resulting d.c. voltage to said second variable-capacitance diode.

6. A frequency synthesizer according to claim 5, wherein said computation means produces said another voltage setup value which is larger than the voltage value data read out of said memory means if the output voltage value of the filter means has a trend of rise, or produces said another voltage setup value which is smaller than the voltage value data read out of said memory means if the output voltage value of said filter means has a trend of fall.

7. A frequency synthesizer according to claim 5 further comprising a temperature sensor which measures the ambient temperature of said VCO, said temperature sensor having an output value delivered to the address line of said memory means.

8. A frequency synthesizer according to claim 7, wherein said memory means stores voltage value data for all channels and in correspondence to temperature values provided by said temperature sensor.

9. A frequency synthesizer comprising a reference signal oscillator which generates a reference signal; a demultiplying phase comparator which compares a signal, that is derived from the output signal through demultiplication by a factor determined by channel data, with the reference signal provided by said reference signal oscillator; a filter means which smoothes the output of said demultiplying phase comparator; a first variable-capacitance diode which varies in the capacitance thereof in response to the output voltage of said filter means; and an oscillator which oscillates at a frequency determined from the capacitance of said first variable-capacitance diode to produce said output signal, wherein said oscillator is connected with said first variable-capacitance diode and a second variable-capacitance diode which determines the oscillation frequency of said oscillator, and wherein said frequency synthesizer further comprises:

a memory means which stores voltage value data indicative of d.c. voltages to be applied to said second variable-capacitance diode in accordance with said channel data;

a voltage detection means which measures the

output voltage of said filter means;

a computation means which modifies voltage value data read out of said memory means in accordance with the output value provided by said voltage detection means at the previous channel switching thereby to produce modified data, and thereafter produces another voltage setup value in accordance with the output value of said voltage detection means; and

a conversion means which converts the voltage setup value provided by said computation means into a d.c. voltage and applies the resulting d.c. voltage to said second variable-capacitance diode.

10. A frequency synthesizer according to claim 9, wherein said memory means stores, for all channels, voltage value data corresponding to voltages to be applied to said second variable-capacitance diode at a certain temperature.

11. A frequency synthesizer according to claim 10, wherein said computation means produces modified data which is larger than the voltage value data read out of said memory means if the output voltage value that is held is larger than a certain reference value, or produces modified data which is smaller than said voltage value data if the output voltage value that is held is smaller than a certain reference value.

12. A frequency synthesizer according to claim 9, wherein said computation means produces said another voltage setup value which is larger than the voltage value data read out of said memory means if the output voltage value of the filter means has a trend of rise, or produces said another voltage setup value which is smaller than the voltage value data read out of said memory means if the output voltage value of said filter means has a trend of fall.

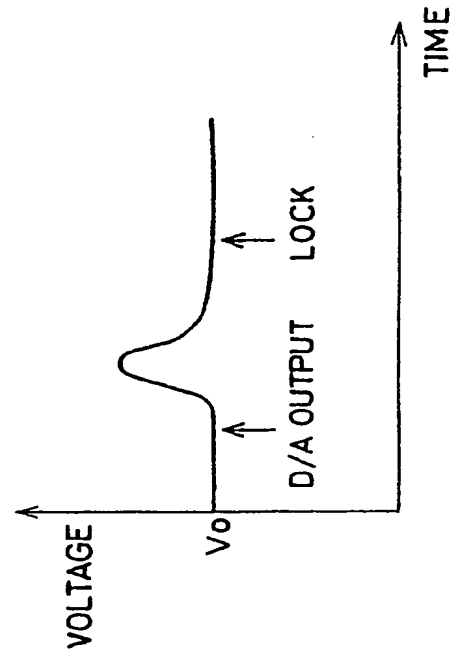
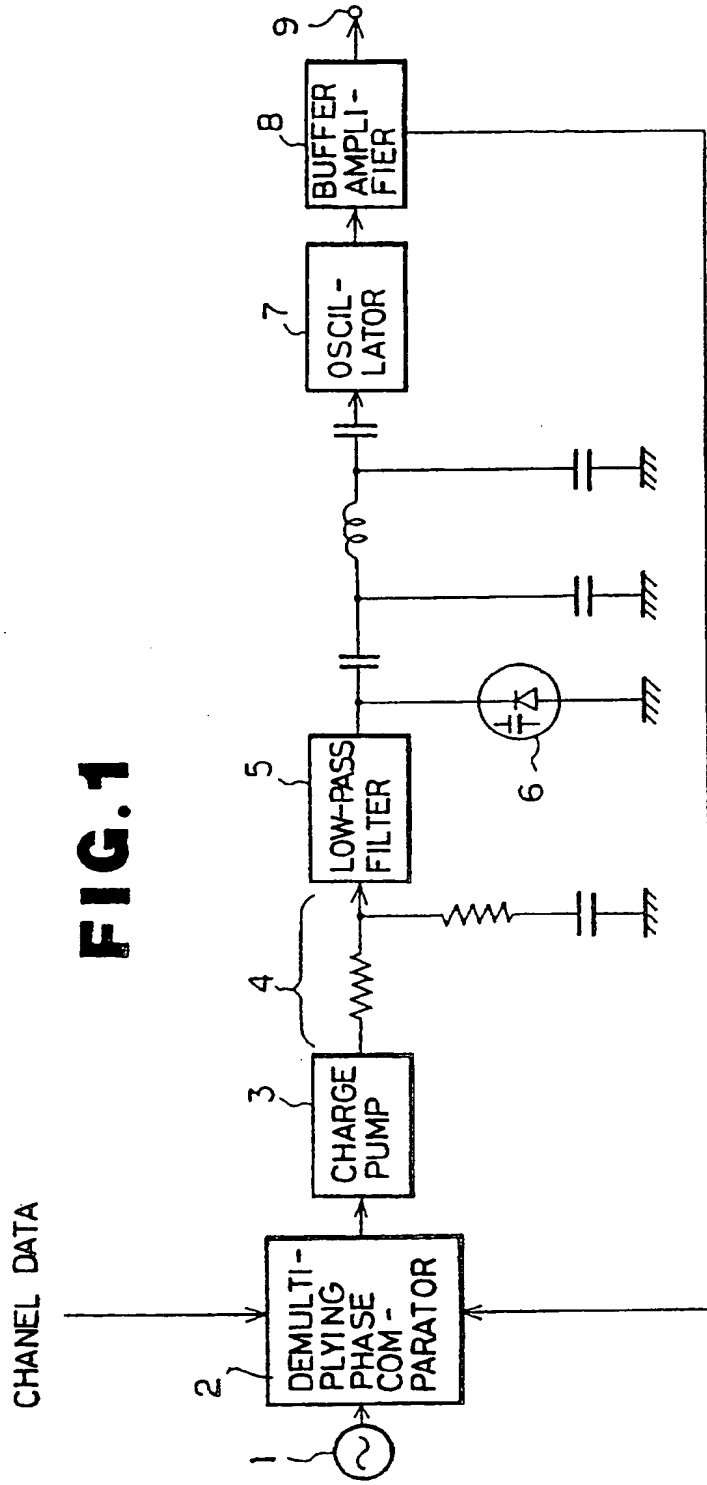


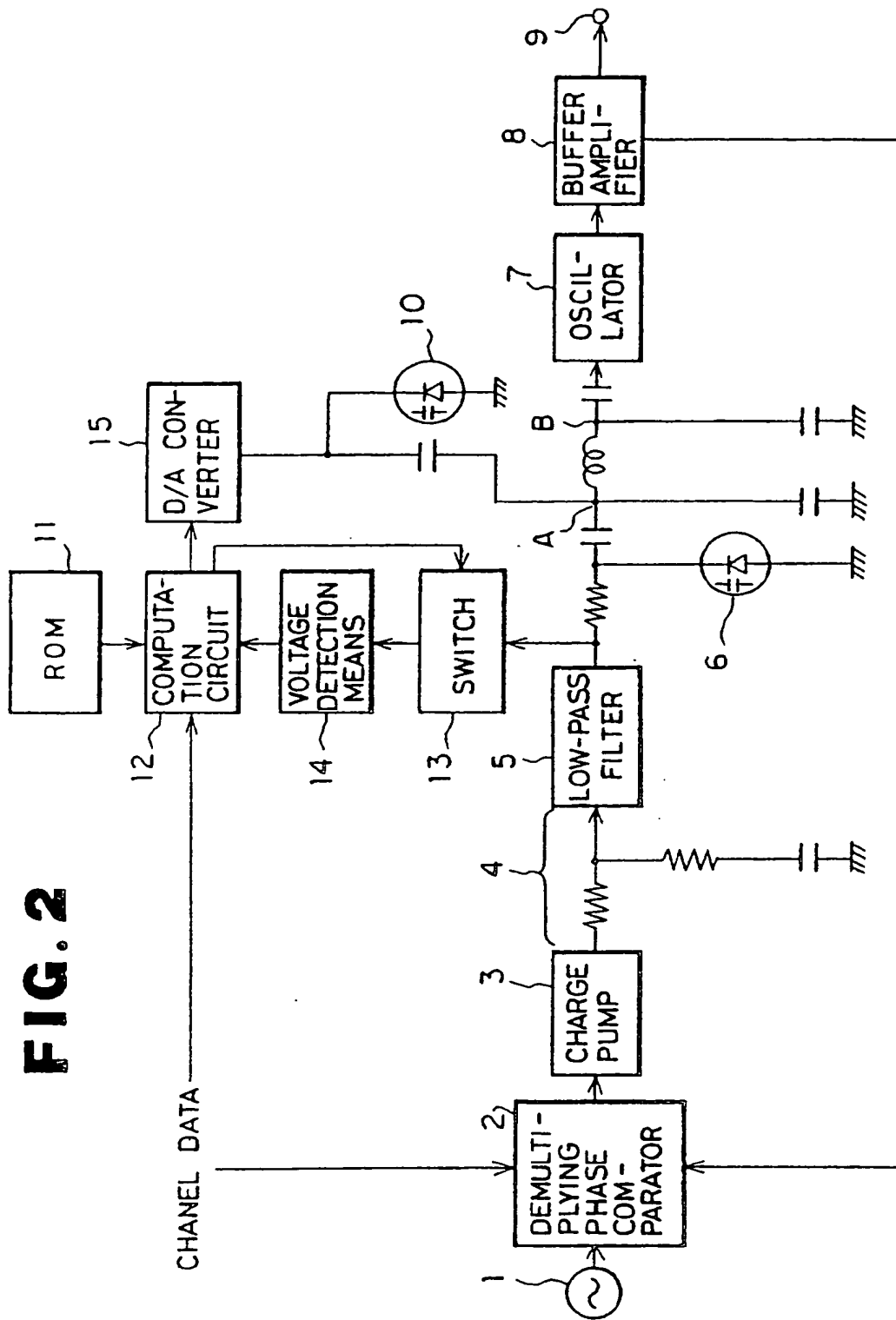
FIG. 2

FIG. 3

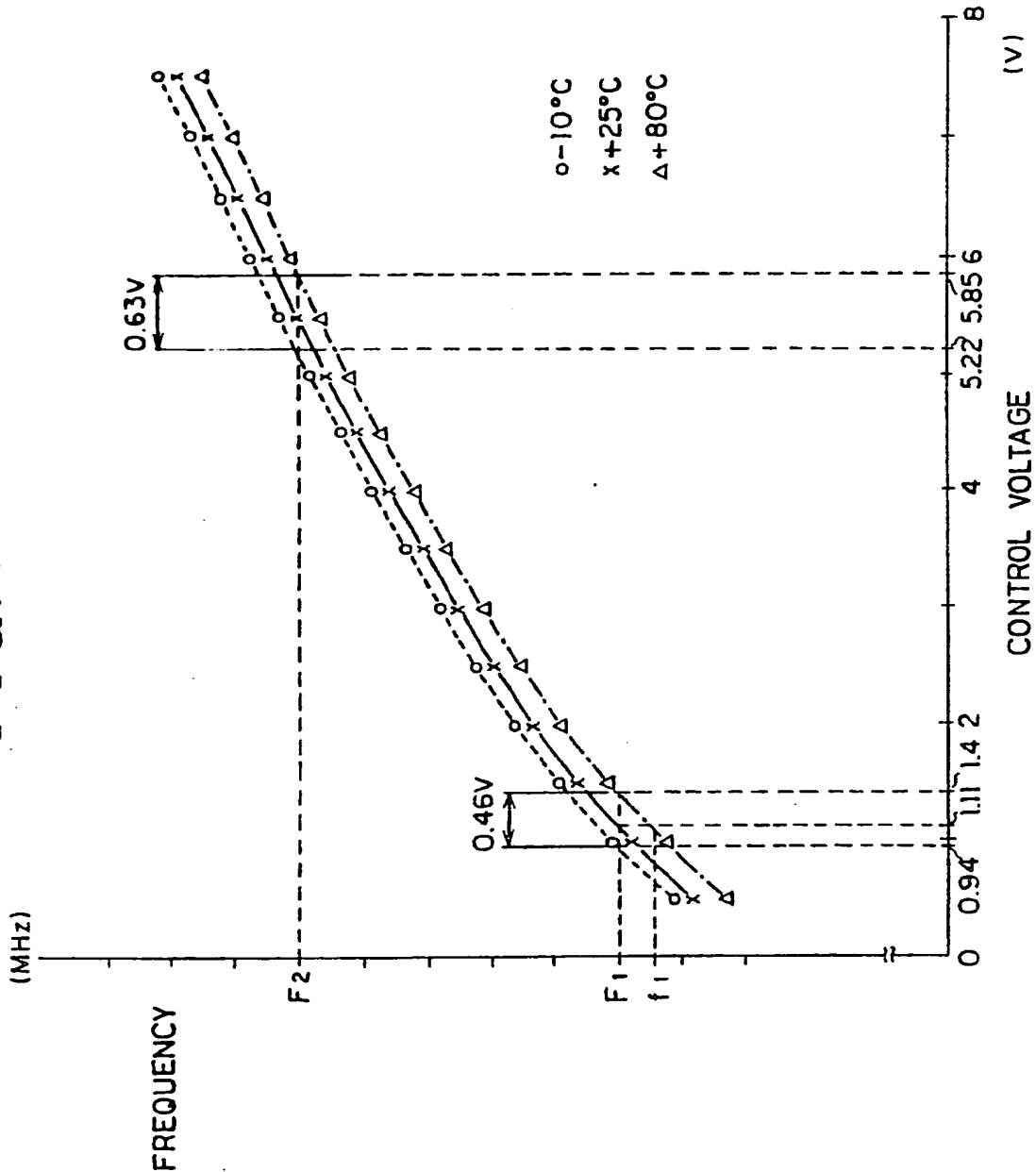


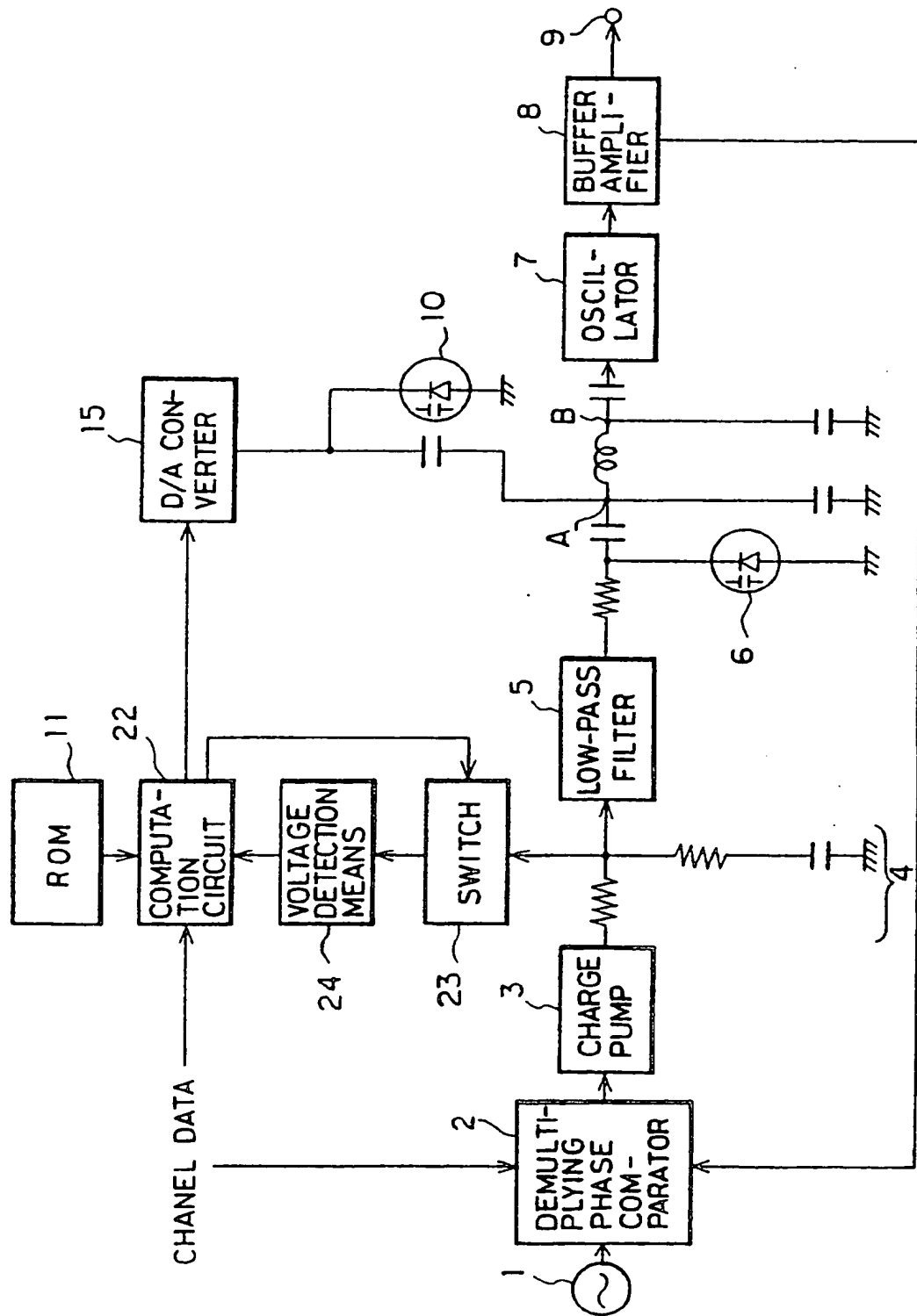
FIG. 5

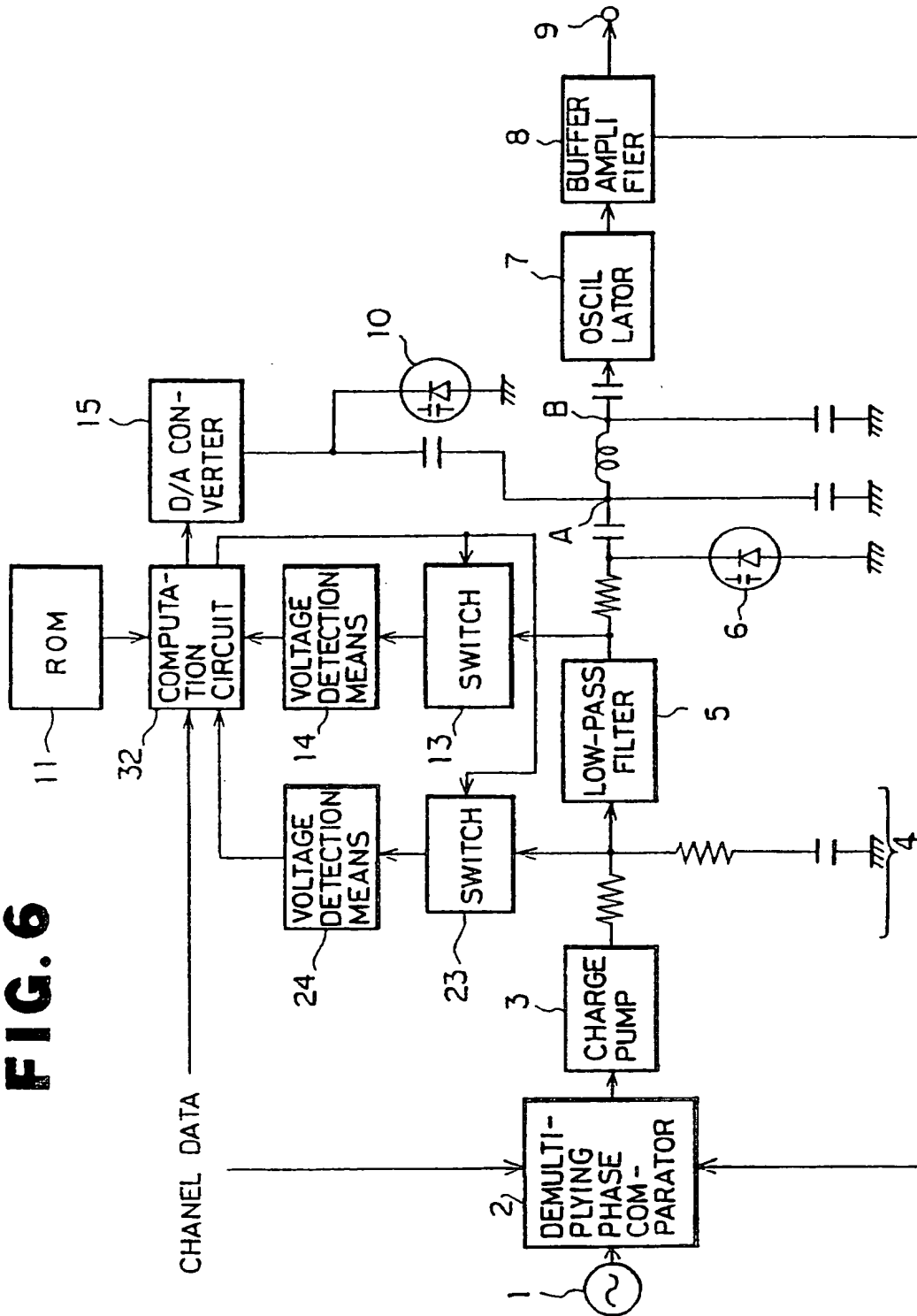
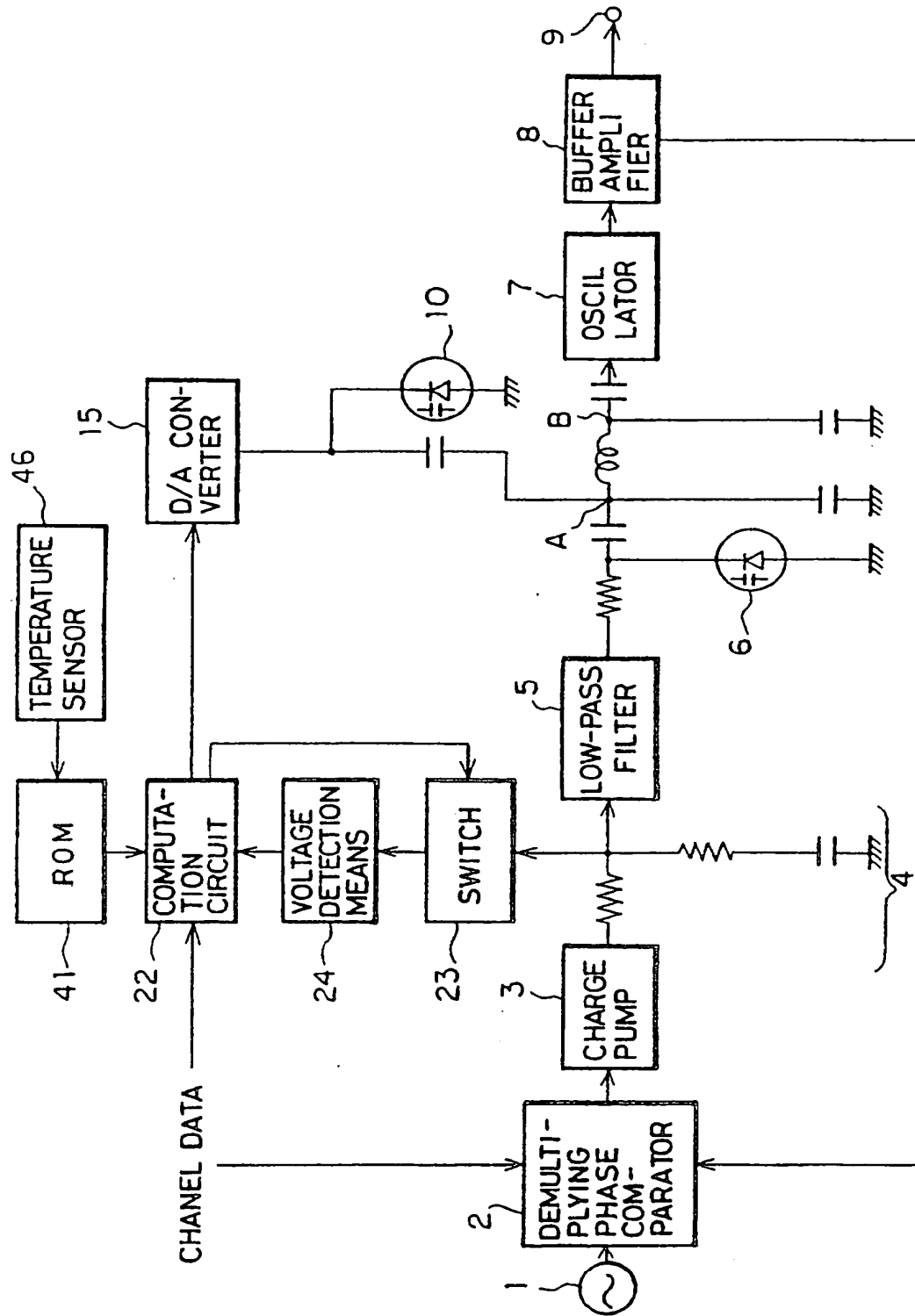
FIG. 6

FIG. 7

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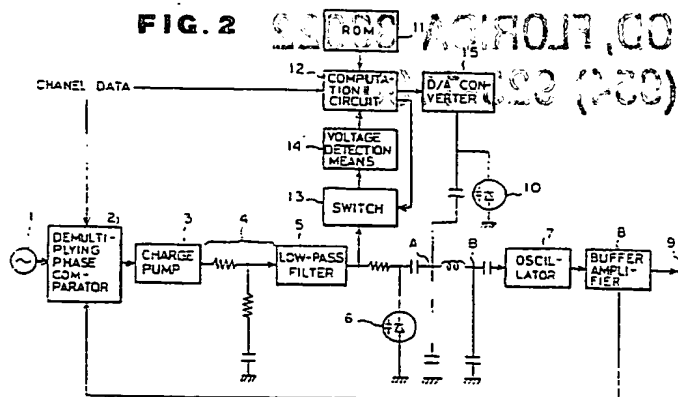
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(54) **Frequency Synthesizer.**

(57) A frequency synthesizer is designed to modify voltage value data read out of a memory means (11) in accordance with the output voltage of a filter means (5), and apply a d.c. voltage corresponding to the modified data to the second variable-capacitance diode (10) in connection with a VCO, thereby allowing the VCO frequency switching without imposing a significant fluctuation of the application voltage to the first variable-capacitance diode and accomplishing a short channel switching time and stable operation

against the temperature fluctuation. The device is further designed to supply a voltage setup value read out of the memory means to the second variable-capacitance diode thereby to reduce the frequency matching time at channel switching, and to determine such another voltage setup value as to reduce the time of phase matching based on the trend of change in the filter output voltage and supply the value to the second variable-capacitance diode.

FIG. 2



European
Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 11 5127

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	FR-A-2 469 823 (THOMSON-CSF) * the whole document * - - -	1-5,7-11	H 03 L 7/14
A,D	PATENT ABSTRACTS OF JAPAN vol. 6, no. 264 (E-150)(1142) December 23, 1982 & JP-A-57 160 227 (FUJITSU K.K.) October 2, 1982 * the whole document * - - -	1,5,9	
X	US-A-4 704 585 (H.V. LIND) * the whole document * - - -	1-5,9-12	
X	EP-A-0 041 882 (THOMSON-CSF) * the whole document * - - -	1,5,9	
X	EP-A-0 210 124 (SIEMENS AKTIENGESELLSCHAFT) * page 2, column 1, line 31 - page 6, column 9, line 10; figures 1-3 * - - -	1,5,9	
X	US-A-4 410 860 (R.W. KIPP ET AL.) * column 1, line 47 - column 5, line 66; figure 1 * - - -	1,5,6	
P,X	EP-A-0 360 442 (NIPPON TELEGRAPH AND TELEPHONE CORPORATION) * the whole document * - - - - -	1,5,9	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H 03 L H 03 J
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The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of search 23 July 91	Examiner DHONDT I.E.E.
CATEGORY OF CITED DOCUMENTS X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document T: theory or principle underlying the invention		E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons ----- &: member of the same patent family, corresponding document	